Design of Electronic code Lock

Hanyue Wang

School of North China Electric Power University, Beijing 100000, China

374589957@qq.com

Keywords: Lock, electronic code, circuit design

Abstract: Locks are commonly used in people's lives. We use the electronic devices to design a code lock. When the correct code is entered, the unlock signal is output to push the actuator action. That the red light is on and the green light is out means the lock is locked. That the green light is on and the red light is out means the lock is open. The red light is on and the buzzer makes a sound indicate the timeout of your unlock action.In the lock control circuit, a modifiable 8421bcd code is stored as a password. When the input code and the lock's preset password are the same, the lock is opened.If the lock is not opened within 5 seconds of the first password input, the circuit enters a self-locking state so that it can no longer be opened and the luminous probe sends out a 10-second warning. The whole system has a reset function.

1. Introduction

Use two sets of switch circuits as input switch circuits and password input circuits, and then use two 4-Bit registers 74ls194, one for the unlock code and the other for the correct password. Using 74ls85 to compare, if the two are equal, a green light unlock signal is formed; If not, a red light signal is formed and the alarm is issued. The light signal lights up the LED indicator with an unlocked signal. The actual circuit requires that the input of the preset cipher circuit is 8421BCD code. If the input is not 8421bcd code, the output display "E" which is completed using the logic relationship of the door. The first action signal with a button switch triggers a five-second timer. If the lock is not opened within 5 seconds, the circuit enters a self-locking state so that it cannot be opened again and the speaker sends out a 10-second alarm signal.

2. Design scheme of each unit circuit

2.1 Design of input switch circuit and input storage circuit

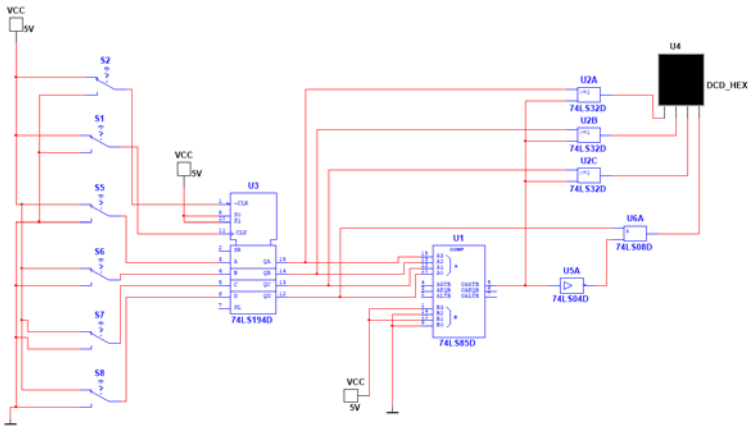

Fig.1 Design of input switch circuit and input storage circuit

2.2 Design of password modification circuit and password storage circuit

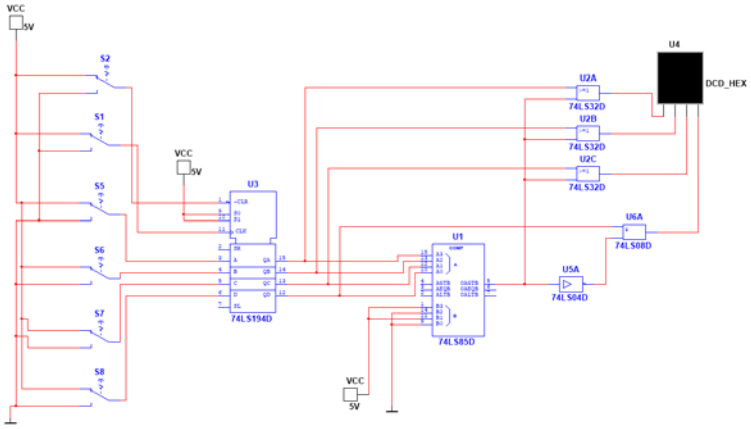

Fig.2 Password modification circuit and password storage circuit diagram

2.3 Design of Compare circuit and display circuit

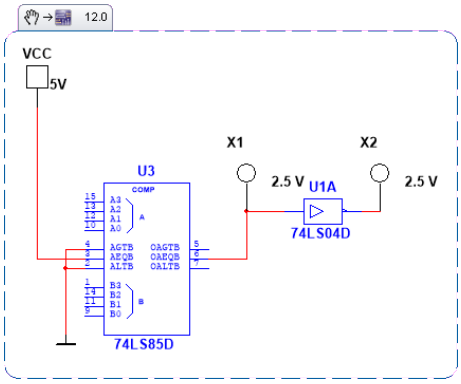

Fig.3 Compare circuit diagram and display circuit diagram

2.4 Design of Time circuit and Sound circuit

The 5s timing circuit is a time interval of 5 1s, so the output is from 0 to 5, and the five-second timing circuit mainly uses the counter 74ls161. The zero-end CLR and the position-end LOAD are placed on the high-power level to make it invalid, and make the energy end ENT, ENP is placed on the high-power level to make it effective. The clock pulse is connected to the CLK signal terminal.

For a five-second timer, when the output is 5, the output QA, QB, QC, and QD are 0, 1, 0, 1. To stop the counter, the clock pulse needs to be set to be invalid. Therefore, the high level signals of QB and QC can be passed through a non-gate and then form an other non-gate with the clock pulse. When the output is 5, the clock pulse CLK end of the chip is always high and there is no pulse. The counter stops working.

The five-second timing circuit is shown in Fig.4.

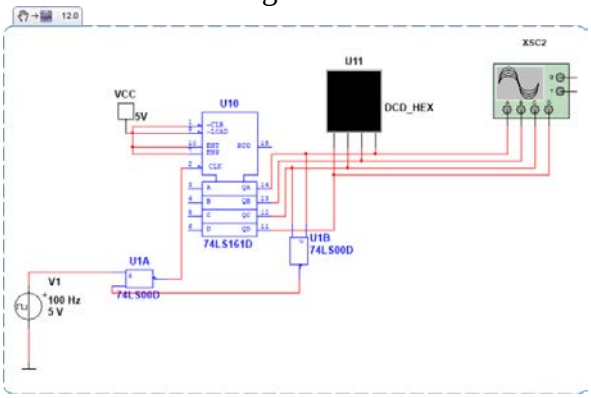

Fig.4 Five-second timing circuit

For the 10s timing circuit, when the output is 10, the QD, QC, QB, and QA are 1,0,1,0. To stop the counter, the clock pulse CLK must be placed invalid. Therefore, the high level signals of QD, QC and QB can be connected through a non-gate and then form an other non-gate with the clock pulse. When the output is 10(displayed as A), the clock pulse CLK end of the chip is always high. There are no more pulses. The counter stops working. The 10-second timing circuit is shown in Figure 5.

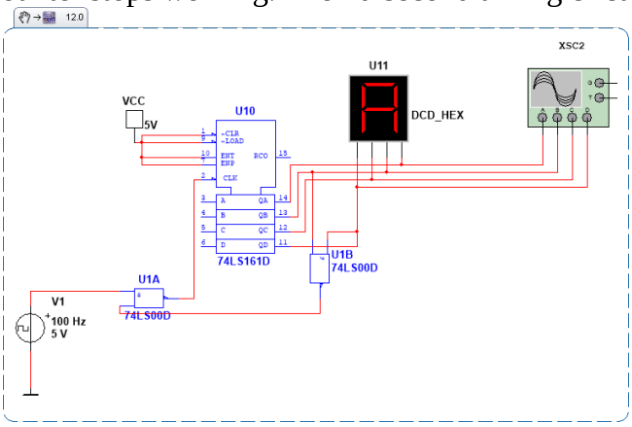

Fig.5 Ten-second timing circuit

When the buzzer ends are high, the buzzer begins to ring; When the buzzer ends are at low power, the buzzer stops making sounds. The sound circuit is shown in Figure 6.

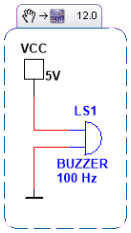

Fig.6 Sound circuit

3. General circuit connection

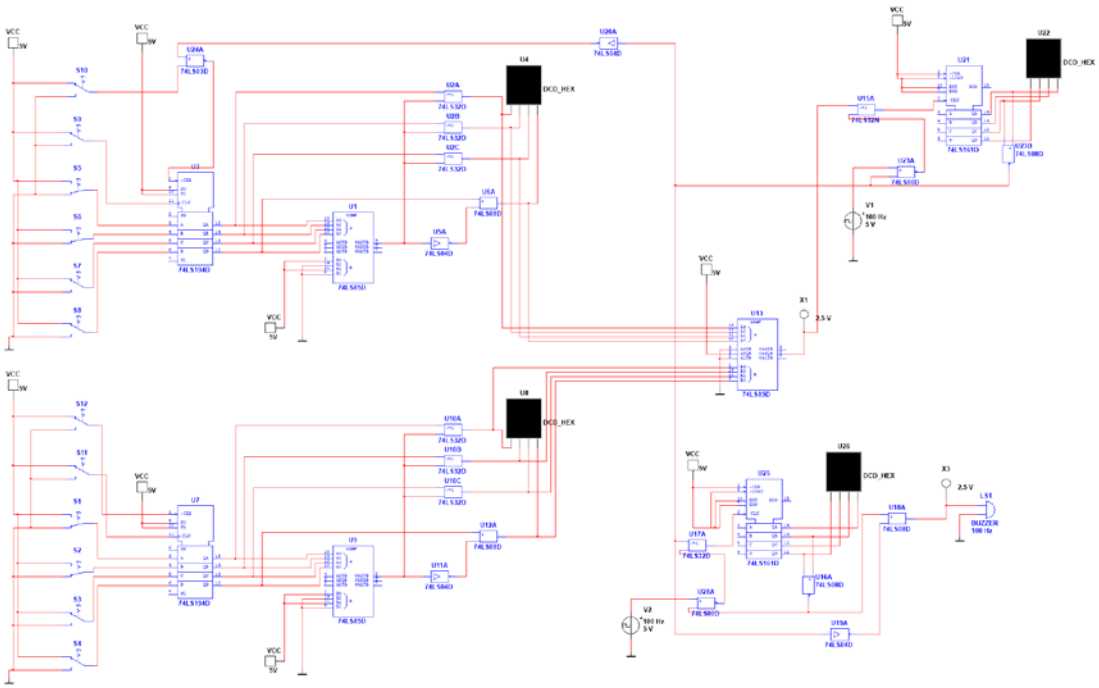

Fig.7 General circuit diagram

4. Conclusion

The input and password circuit realizes the preset password and input code setting and locking through the switch and two pieces of 74ls194. The logic gate guarantees that the input is displayed as E when it is not the 8421bcd code; The result of unlocking or unlocking is given after comparing the input value with the preset password value by Compare and display circuits. The timing circuit sets a delay of 5 seconds and 10 seconds for the circuit. If the lock is not opened within 5 seconds after the first password input, the circuit enters a self-locking state so that it cannot be opened again, and the speaker emits 10 seconds. Sound circuit analog alarm signal.

References

[1] Shuyan Sun. Guide to Electronic Technology Comprehensive Experiments[M] . Beijing: Higher Education Press. 2015.9.

[2] Liuyun, Shuyan Sun, Xiaoming Huang, Zhaodong, Chunying Liu.Digital Electronics Experimental Guide. Second Edition. China Electric Power Publishing House. 2017.11.

[3] Weijing Liu, Zengqiang Liu, Chunming Wang, Yangyv, Yanru Yv.Simulated Electronic Technology Foundation.Tsinghua University Press.2018.3

[4] Kouge, Liping Jiang.Analog and Digital Circuits.Electronic Industry Press.2019.8